(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 298 793 A1

(12) **EUROPEAN PATENT APPLICATION**
published in accordance with Art. 158(3) EPC

(43) Date of publication:
02.04.2003 Bulletin 2003/14

(21) Application number: **01943885.2**

(22) Date of filing: **29.06.2001**

(51) Int Cl.[7]: **H03F 3/19**

(86) International application number:
PCT/JP01/05667

(87) International publication number:
WO 02/003546 (10.01.2002 Gazette 2002/02)

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **30.06.2000 WOPCT/JP00/04367**

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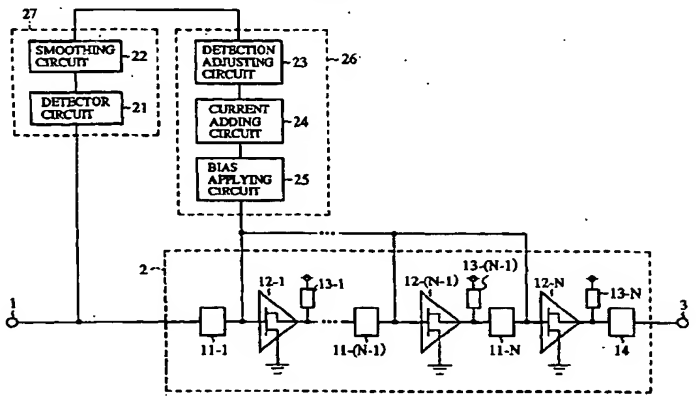
(54) HIGH-FREQUENCY AMPLIFIER

(57) A high-frequency amplifying unit 2 in which a steep gain variation developed according to a change in the amplitude of input high-frequency signal is suppressed is provided. It amplifies an input high-frequency signal with a plurality of transistors 12-1 to 12-N at the same time a measuring circuit 27 measures amplitude of the input high-frequency signal, and a bias control circuit 26 continuously controls a bias applied to each transistors 12-1 to 12-N according to the value of amplitude measured by the measuring circuit 27. Thus it is possible to suppress a steep gain variation produced according to a variation in the amplitude of input high-frequency signal.

FIG.2



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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a high-frequency amplifying device which is used in, for example, a mobile communication terminal to amplify a high-frequency signal.

Description of the Rior Art

[0002] Fig. 1 is a block diagram showing a configuration of conventional high-frequency amplifying device described in, for example, "Intelligent RF Power Module Using Automatic Bias Control (ABC) System for PCS CDMA Applications" (Sato et al., IEEE MTT-S Int. Microwave Symp. Dig. p.p.201-204, 1998). In the figure, reference numeral 201 indicates an input terminal, 202-1 indicates a first-stage transistor for amplifying a high-frequency signal, and 202-2 indicates a second-stage transistor for amplifying the high-frequency signal. 203-1 indicates a bias feed circuit such as a distributed constant circuit, a resistor, an inductor, a capacitor or the like for biasing the input of transistor 202-1, and 203-2 indicates a bias feed circuit for biasing the input of transistor 202-2. 204-1 indicates a pull-up circuit provided on the output side of transistor 202-1, 204-2 indicates a pull-up circuit provided on the output side of transistor 202-2, and 205 indicates an output terminal, respectively.

[0003] In addition, reference numeral 211 indicates a transistor for detecting an input signal, 212 indicates a pull-up circuit on the output side of transistor 211, and 213 indicates a comparator for comparing a reference voltage generated by a reference voltage source 214 and a voltage of signal detected by the transistor 211. 214 indicates a reference voltage source for generating a predetermined reference voltage, and 215 indicates a variable voltage source for applying a voltage corresponding to the result of comparison by the comparator 213 to each bias feed circuits 203-1 and 203-2.

[0004] The operation will next be explained.

[0005] A high-frequency signal supplied via the input terminal 201 is amplified by the transistors 202-1 and 202-2 and the post-amplification high-frequency signal is output through the output terminal 205.

[0006] On the other hand, the transistor 211 detects the high-frequency signal supplied via the input terminal 201 and supplies a post-detection signal to the comparator 213. The comparator 213 compares a reference voltage generated by the reference voltage source 214 and a voltage of signal detected by the transistor 211 and supplies a signal (e.g., a signal of 0 or 1) indicative of whether the voltage of post-detection signal is higher than the reference voltage, to a variable voltage source 215. The variable voltage source 215 changes the voltage to apply to each bias feed circuits 203-1 and 203-2 according to whether or not the voltage of input signal is higher than the reference voltage.

[0007] Thus the biases to be applied to the transistors 202-1 and 202-2 are changed according to the voltage (power) of input signal to reduce power consumption at low output power.

[0008] However, because the conventional high-frequency amplifying device is constructed as described above, it has been accompanied by problems that a variation in gain at their changing is large and, for example, further reduction in power consumption is difficult, since the biases to be applied to the transistors are changed discontinuously based on whether or not the voltage of input signal is higher than the reference voltage. There was a possibility that when the variation in gain at the changing was large, a shift occurred in the phase of a signal, thus causing defective conditions upon detection. When a system, such as a W-CDMA (Wideband Code Division Multiple Access) system which is placed under strict constraints on a gain fluctuation band width, is used in a communication apparatus or the like, it has been difficult to meet such constraints when the gain variation at the changing is large.

[0009] The present invention has been made to solve the foregoing problems. Therefore the present invention aims to provide a high-frequency amplifying device comprising a high-frequency amplifying unit having a plurality of the amplifying elements for amplifying the input high-frequency signal; a measuring circuit for measuring amplitude of the input high-frequency signal; and a bias control circuit for continuously controlling a bias applied to each amplifying elements according to value of the amplitude measured by the measuring circuit, whereby a steep gain variation developed according to a change in the amplitude of input high-frequency signal can be suppressed.

SUMMARY OF THE INVENTION

[0010] According to a first aspect of the present invention, a high-frequency amplifying device comprises: a high-frequency amplifying unit having a plurality of the amplifying elements for amplifying the input high-frequency signal; a measuring circuit for measuring amplitude of the input high-frequency signal; and a bias control circuit for continuously controlling a bias applied to each amplifying elements according to value of the amplitude measured by the measuring circuit. By this arrangement, an effect is obtained that a steep gain variation developed according to a change in the amplitude of input high-frequency signal can be suppressed. Further, another effect is obtained that the circuit scale can be reduced since the bias control circuit collectively controls bias applied to the plurality of amplifying elements.

[0011] According to a second aspect of the present invention, a high-frequency amplifying device in which bias control circuit has a current adding circuit for out-

putting a current having a value corresponding to the amplitude measured by the measuring circuit, and a bias applying circuit for applying a bias corresponding to the sum of current output from the current adding circuit and a predetermined reference current to the plurality of amplifying elements is provided. By this arrangement an effect is obtained that the bias can be reduced continuously and power consumption at low output power can be further reduced when the amplitude of input high-frequency signal becomes small.

[0012] According to a third aspect of the present invention, a high-frequency amplifying device in which bias control circuit has a detection adjusting circuit for setting value of a current conducted according to the amplitude of the high-frequency signal when the measuring circuit measures the amplitude thereof is provided. By this arrangement an effect is obtained that an operating condition for the measuring circuit can be controlled and an adjustment of the device can be carried out with ease.

[0013] According to a fourth aspect of the present invention, a high-frequency amplifying device in which current adding circuit has a current mirror circuit for allowing a current having a value corresponding to the amplitude measured by the measuring circuit to conduct into one end thereof and according to the current, outputting another current set based on a ratio between junction areas of the current mirror circuit and a source voltage from the other end thereof is provided. By this arrangement an effect is obtained that the characteristic of current to the bias applying circuit with respect to the amplitude of input high-frequency signal can easily be adjusted by adjusting the ratio between the junction areas of current mirror circuit and the source voltage thereof, and in its turn the bias applied to each amplifying elements can be adjusted with ease.

[0014] According to a fifth aspect of the present invention, ahigh-frequency amplifying device in which bias applying circuit has an internal amplifying element for conducting the current output from the current adding circuit and the predetermined reference current, and the internal amplifying element and the plurality of amplifying elements of the high-frequency amplifying unit constitute a current mirror circuit is provided.

[0015] According to a sixth aspect of the present invention, a high-frequency amplifying device in which bias control circuit has a current subtracting circuit for inputting thereto a current having a value corresponding to the amplitude measured by the measuring circuit, and a bias applying circuit for supplying the current to the current subtracting circuit and applying a bias corresponding to a difference between a predetermined reference current and said current to the plurality of amplifying elements is provided. By this arrangement an effect is obtained that it is possible to continuously increase the bias when the input high-frequency signal is reduced in amplitude, and thereby compensate for a gain reduction at low output power.

[0016] According to a seventh aspect of the present invention, a high-frequency amplifying device in which bias control circuit has a detection adjusting circuit for setting a value of current conducted according to the amplitude of high-frequency signal when the measuring circuit measures the amplitude thereof is provided. By this arrangement an effect is obtained that the operating condition for measuring circuit can be controlled, and hence an adjustment of the device can easily be performed.

[0017] According to an eighth aspect of the present invention, a high-frequency amplifying device in which current subtracting circuit has a current mirror circuit for allowing a current having a value corresponding to the amplitude measured by the measuring circuit to conduct into one end thereof and according to the current, inputting another current set based on a ratio between junction areas of the current mirror circuit and a source voltage from the other end thereof is provided. By this arrangement an effect is obtained that the characteristic of current from the bias applying circuit with respect to the amplitude of input high-frequency signal can easily be adjusted by adjusting the ratio between the junction areas of current mirror circuit and the source voltage thereof, and in its turn the bias applied to each amplifying elements can be adjusted with ease.

[0018] According to a ninth aspect of the present invention, a high-frequency amplifying device in which bias applying circuit has an internal amplifying element for conducting the remaining current obtained by subtracting the current supplied to the current subtracting circuit from the predetermined reference current, and the internal amplifying element and the plurality of amplifying elements of the high-frequency amplifying unit constitute a current mirror circuit is provided.

[0019] According to a tenth aspect of the present invention, a high-frequency amplifying device in which measuring circuit is connected in parallel with the high-frequency amplifying unit is provided. By this arrangement an effect is obtained that the amplitude of high-frequency signal can be measured without degradation of the high-frequency signal supplied to the high-frequency amplifying unit.

[0020] According to an eleventh aspect of the present invention, a high-frequency amplifying device in which measuring circuit, current adding circuit and detection adjusting circuit are connected in parallel with the high-frequency amplifying unit is provided. By this arrangement an effect is obtained that the measuring circuit, the detection adjusting circuit and the current subtracting circuit can be implemented in a one-chip integrated circuit, thus it makes possible to reduce the scale and cost of the device.

[0021] According to a twelfth aspect of the present invention, a high-frequency amplifying device in which measuring circuit, current subtracting circuit and detection adjusting circuit are connected in parallel with high-frequency amplifying unit is provided. By this arrange-

ment an effect is obtained that the measuring circuit, the detection adjusting circuit and the current subtracting circuit can be implemented in a one-chip integrated circuit, thus it makes possible to reduce the scale and cost of the device.

[0022] According to a thirteenth aspect of the present invention, a high-frequency amplifying device in which measuring circuit has a detector circuit connected in series with the high-frequency amplifying unit, for passing the high-frequency signal to the high-frequency amplifying unit and detecting the high-frequency signal is provided. By this arrangement an effect is obtained that it is not necessary to additionally provide a divider for allowing the high-frequency signal to divide into the measuring circuit and the high-frequency amplifying unit, and hence a circuit scale can be reduced.

[0023] According to a fourteenth aspect of the present invention, a high-frequency amplifying device comprises: a high-frequency amplifying unit having a plurality of the amplifying elements for amplifying the input high-frequency signal; a measuring circuit for measuring the amplitude of input high-frequency signal; and a plurality of bias control circuits for respectively independently controlling continuously biases applied to the respective amplifying elements according to the value of amplitude measured by the measuring circuit. By this arrangement an effect is obtained that the biases can independently be set according to the frequency characteristics and physical characteristics of the respective amplifying elements, for example.

[0024] According to a fifteenth aspect of the present invention, a high-frequency amplifying device in which each bias control circuits has a current adding circuit for outputting a current having a value corresponding to the amplitude measured by the measuring circuit, and a bias applying circuit for applying a bias corresponding to the sum of current output from the current adding circuit and a predetermined reference current to the each amplifying element is provided. By this arrangement an effect is obtained that the power consumption at low output power can be further reduced since the biases applied to the respective amplifying elements can be established independently.

[0025] According to a sixteenth aspect of the present invention, a high-frequency amplifying device in which each bias control circuit has a current subtracting circuit for inputting thereto a current having a value corresponding to the amplitude measured by the measuring circuit, and a bias applying circuit for supplying the current to the current subtracting circuit and applying a bias corresponding to the difference between a predetermined reference current and the current to the each amplifying element is provided. By this arrangement an effect is obtained that the compensation for a gain reduction at low output power can be carried out more suitably since the biases for the respective amplifying elements can be set independently.

[0026] According to a seventeenth aspect of the present invention, a high-frequency amplifying device in which each bias control circuit of a predetermined number of stages on the front side, of the plurality of bias control circuits has a current subtracting circuit for inputting thereto a current having a value corresponding to the amplitude measured by the measuring circuit, and a bias applying circuit for supplying the current to the current subtracting circuit and applying a bias corresponding to the difference between a predetermined reference current and the supplied current to the each amplifying element, and each remaining bias control circuits on the rear side has a current adding circuit for outputting a current having a value corresponding to the amplitude measured by the measuring circuit, and a bias applying circuit for applying a bias corresponding to the sum of current output from the current adding circuit and a predetermined reference current to the each amplifying element is provided. By this arrangement an effect is obtained that a reduction in distortion and a reduction in power consumption at low output power can be rendered compatible.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027]

Fig. 1 is a block diagram showing a configuration of conventional high-frequency amplifying device;

Fig. 2 is a block diagram showing a configuration of high-frequency amplifying device according to an embodiment 1 of the present invention;

Fig. 3 is a circuit diagram showing an example of configuration of a detection adjusting circuit shown in Fig. 2;

Fig. 4 is a circuit diagram showing an example of configuration of a current adding circuit shown in Fig. 2;

Fig. 5 is a circuit diagram showing an example of configuration of a bias applying circuit shown in Fig. 2;

Fig. 6 is a block diagram showing a configuration of high-frequency amplifying device according to an embodiment 2 of the present invention;

Fig. 7 is a circuit diagram showing configurations of a detection adjusting circuit and a current subtracting circuit shown in Fig. 6;

Fig. 8 is a block diagram showing a configuration of high-frequency amplifying device according to an embodiment 3 of the present invention;

Fig. 9 is a block diagram showing a configuration of high-frequency amplifying device according to an embodiment 4 of the present invention;

Fig. 10 is a block diagram showing a configuration of high-frequency amplifying device according to an embodiment 5 of the present invention;

Fig. 11 is a block diagram showing a configuration of high-frequency amplifying device according to an embodiment 6 of the present invention; and

Fig. 12 is a circuit diagram showing an example of configuration of a detector circuit shown in Fig. 11.

DETAILED DESCRIPTION OF THE PREFERED EMBODIMENT

[0028] In order to describe the present invention in more details, best modes for carrying out the present invention will hereinafter be described with reference to the accompanying drawings.

Embodiment 1

[0029] Fig. 2 is a block diagram showing a configuration of high-frequency amplifying device according to an embodiment 1 of the present invention. In the figure, reference numeral 1 indicates an input terminal, 2 indicates a high-frequency amplifying unit having transistors 12-1 to 12-N of N stages (where $N \geqq 2$), and 3 indicates an output terminal.

[0030] In the high-frequency amplifying unit 2, reference numerals 11-1 to 11-N respectively indicate matching circuits. respectively provided at stages prior to the transistors, and 12-1 to 12-N, 12-1 to 12-N respectively indicate the transistors of N stages (amplifying elements) for amplifying a RF or high-frequency signal. 13-1 to 13-N respectively indicate pull-up circuits provided at the outputs of transistors 12-1 to 12-N, and 14 indicates a matching circuit provided at a stage prior to the output terminal 3, respectively.

[0031] Reference numeral 21 indicates a detector circuit such as a diode for detecting an input signal, and 22 indicates a smoothing circuit such as a capacitor for smoothing a post-detection signal. Incidentally, the detector circuit 21 and the smoothing circuit 22 constitute a measuring circuit 27 for measuring the amplitude of input signal.

[0032] Reference numeral 23 indicates a detection adjusting circuit for adjusting or regulating a current passing through the detector circuit 21 and the smoothing circuit 22, 24 indicates a current adding circuit for supplying a current of value corresponding to the amplitude of input signal to a bias applying circuit 25, based on the current adjusted by the detection adjusting circuit 23, and 25 indicates a bias applying circuit for adding the current supplied from the current adding circuit 24 to a reference current and applying a bias corresponding to the post-addition current to the bases of transistors 12-1 to 12-N, respectively. Incidentally, the detection adjusting circuit 23, the current adding circuit 24, and the bias applying circuit 25 constitute a bias control circuit 26.

[0033] Examples of configurations of the detection adjusting circuit 23, the current adding circuit 24 and the bias applying circuit 25 at the time that N type bipolar transistors are used as the transistors 12-1 to 12-N, will now be shown. Fig. 3 is a circuit diagram showing an example of configuration of the detection adjusting circuit 23 shown in Fig. 2, Fig. 4 is a circuit diagram showing an example of configuration of the current adding circuit 24, and Fig. 5 is a circuit diagram showing an example of configuration of the bias applying circuit 25.

[0034] In the detection adjusting circuit 23 shown in Fig. 3, reference numeral 31 indicates a variable resistor provided between an N type transistor 32 and a smoothing circuit 22, 32 and 33 respectively indicate the N type transistors constituting a current mirror circuit whose one end is connected to the variable resistor 31 and other end is connected to the current adding circuit 24, and 34 indicates a power supply connected to the collector and base of the N type transistor 32 and the base of N type transistor 33. Incidentally, a current mirror circuit conducts a current through one end thereof and the other end thereof at the same ratio as a ratio between junction areas of transistors, an N type transistor-based current mirror circuit allows currents to flow in from one end thereof and the other end thereof, and a P type transistor-based current mirror circuit allows currents to flow out from one end thereof and the other end thereof. The detector circuit 21 comprises a diode D as shown in Fig. 3 by way of example, and the smoothing circuit 22 is made up of a capacitor C as shown in Fig. 3 by way of example. Incidentally, the capacitance value of capacitor C is set according to a chip rate of the high-frequency signal, etc. The capacitor C serves so as to smooth a post-detection signal and suppresses the flowing of high-frequency signal into the bias control circuit 26.

[0035] In the current adding circuit 24 shown in Fig. 4, reference numerals 41 and 42 respectively indicate P type transistors that constitute a current mirror circuit whose one end is connected to the detection adjusting circuit 23 and whose other end is connected to the bias applying circuit 25, and reference numeral 43 indicates a power supply connected to the emitters of P type transistors 41 and 42.

[0036] In the bias applying circuit 25 shown in Fig. 5, reference numeral 51 indicates an N type transistor (internal amplifying element) whose collector is connected to the current adding circuit 24 and whose emitter is grounded, 52 indicates a resistor provided between the collector of N type transistor 51 and a power supply 53, 53 indicates the power supply, 54 indicates an N type transistor whose base is connected to the collector of N type transistor 51 and whose emitter is connected to the base of N type transistor 51, 55 indicates a resistor provided between the collector of N type transistor 54 and the power supply 53, 56 indicates a capacitor, and 57 indicates an inductor which is provided between the base of N type transistor 51 and the bases of transistors 12-1 to 12-N of the high-frequency amplifying unit 2 to suppress the flowing of a high-frequency signal from the high-frequency amplifying unit 2, respectively. Incidentally, the N type transistor 51 constitutes a current mirror circuit together with the N type transistors 12-1 to 12-N of the high-frequency amplifying unit 2.

[0037] The operation will next be explained.

[0038] The high-frequency signal supplied via the input terminal 1 is amplified by the transistors 12-1 to 12-N of the high-frequency amplifying unit 2 and the amplified high-frequency signal is output through the output terminal 3.

[0039] On the other hand, the detector circuit 21 detects the high-frequency signal supplied via the input terminal 1 and supplies the post-detection signal to the smoothing circuit 22. The smoothing circuit 22 smoothes the signal. Incidentally, the detection adjusting circuit 23 connected to the smoothing circuit 22 adjusts a current passing through the detector circuit 21 and the smoothing circuit 22. The current adding circuit 24 supplies a current of value corresponding to the amplitude of input signal to the bias applying circuit 25, based on the current adjusted by the detection adjusting circuit 23. The bias applying circuit 25 adds the current supplied from the current adding circuit 24 to a reference current and applies a bias corresponding to the so-added current to the bases of transistors 12-1 to 12-N. Thus when the amplitude of input signal increases, the post-addition current increases and the bias applied to each bases of transistors 12-1 to 12-N becomes large. On the other hand, when the amplitude of input signal decreases, the post-addition current is reduced and the bias applied to each base of transistors 12-1 to 12-N decreases.

[0040] A description will now be made of operation at the time that the respective parts are configured as shown in Figs. 3 through 5.

[0041] First, the detector circuit 21 and the smoothing circuit 22 extract the voltage amplitude of an input signal and allow a current corresponding to the voltage amplitude of input signal to conduct into the N type transistor 32 of current mirror circuit, based on the resistance value of variable resistor 31 and the voltage of power supply 34. Thus a current obtained by multiplying the current by a ratio between junction areas of the N type transistors 32 and 33 is allowed to conduct into the N type transistor 33 of current mirror circuit (see Fig. 3).

[0042] The same current is caused to conduct even into the P type transistor 41 of current mirror circuit in the current adding circuit 24, which is connected to the N type transistor 33. Thus a current having a value obtained by multiplying the current by a ratio between junction areas of the P type transistors 41 and 42 is allowed to conduct into the P type transistor 42 of current mirror circuit (see Fig. 4).

[0043] In the bias applying circuit 25, a reference bias for the N type transistor 51 is determined according to a voltage from the power supply 53, a resistance value of the resistor 52 and an emitter-to-base voltage of the N type transistor 54 when no current is supplied from the current adding circuit 24. A reference current corresponding to the reference bias serves so as to make continuity between the collector and emitter. When the current is supplied from the current adding circuit 24, the current is added to the reference current, followed by flowing into the collector of N type transistor 51 of the bias applying circuit 25. The bias applied to the base of N type transistor 51 also varies according to the change in the emitter-to-collector current. Since the N type transistor 51 constitutes the current mirror circuit together with the transistors 12-1 to 12-N of high-frequency amplifying unit 2, the bias applied to each bases of transistors 12-1 to 12-N of the high-frequency amplifying unit 2 also changes in the same manner as described above (see Fig. 5).

[0044] Thus the detector circuit 21, the smoothing circuit 22, the detection adjusting circuit 23, the current adding circuit 24 and the bias applying circuit 25 continuously adjust the bias for each transistors 12-1 to 12-N of high-frequency amplifying unit 2 according to the amplitude of input signal.

[0045] Thus according to the embodiment 1, an effect is obtained that a steep gain variation produced according to a change in the amplitude of input high-frequency signal can be suppressed, since the high-frequency amplifying unit 2 having the plurality of transistors 12-1 to 12-N for amplifying the input high-frequency signal, the measuring circuit 27 for measuring the amplitude of input high-frequency signal, and the bias control circuit 26 for continuously controlling the bias applied to each transistors 12-1 to 12-N according to the value of amplitude measured by the measuring circuit 27 are provided.

[0046] According to the embodiment 1 as well, an effect is obtained that the circuit scale can be reduced since the bias control circuit 26 collectively controls the bias applied to each plurality of transistors 12-1 to 12-N.

[0047] Further according to the embodiment 1, an effect is obtained that the bias can be lowered continuously when the amplitude of input high-frequency signal is reduced, thus it makes possible to further reduce power consumption at low output power since the bias control circuit 26 has the current adding circuit 24 for outputting the current having a value corresponding to the amplitude measured by the measuring circuit 27, and the bias applying circuit 25 for applying the bias corresponding to the sum of current from the current adding circuit 24 and the predetermined reference current to each transistors 12-1 to 12-N.

[0048] Furthermore according to the embodiment 1, an effect is obtained that an operating condition (operating point of the diode constituting the detector circuit 21) for the measuring circuit 27 can be controlled and hence an adjustment of the device can be easily performed since the bias control circuit 26 has the detection adjusting circuit 23 for setting a value of current conducted or carried according to the amplitude of high-frequency signal when the measuring circuit 27 measures the amplitude.

[0049] Still further according to the embodiment 1, an effect is obtained that the characteristic of current to the bias applying circuit 25 with respect to the amplitude of input high-frequency signal can easily be adjusted by adjusting the ratio between the junction areas of current mirror circuit and the source voltage thereof, and in its

turn the bias applied to each transistors 12-1 to 12-N can be adjusted with ease since the current adding circuit 24 has the current mirror circuit for allowing the current of value corresponding to the amplitude measured by the measuring circuit to conduct into one end thereof and outputting the current set based on the ratio between the junction areas of current mirror circuit and the source voltage thereof from the other end thereof according to the above current.

[0050] Still further according to the embodiment 1, an effect is obtained that the measuring circuit 27 is capable of measuring the amplitude of high-frequency signal without degradation of the high-frequency signal supplied to the high-frequency amplifying unit 2 since the measuring circuit 27 is connected in parallel with the high-frequency amplifying unit 2.

[0051] Still further according to the embodiment 1, an effect is obtained that the measuring circuit 27, the detection adjusting circuit 23 and the current adding circuit 24 can be implemented in a one-chip integrated circuit, thus it makes possible to reduce the scale and cost of the device since the measuring circuit 27, the detection adjusting circuit 23 and the current adding circuit 24 are connected in parallel with the high-frequency amplifying unit.

Embodiment 2

[0052] Fig. 6 is a block diagram showing a configuration of high-frequency amplifying device according to an embodiment 2 of the present invention. In the figure, reference numeral 61 indicates a detection adjusting-circuit for adjusting a current passing through a detector circuit 21 and a smoothing circuit 22, and 62 indicates a current subtracting circuit for causing a current having a value corresponding to the amplitude of an input signal to be supplied from a bias applying circuit 25 based on the current adjusted by the detection adjusting circuit 23. Incidentally, the detection adjusting circuit 61, the current subtracting circuit 62 and the bias applying circuit 25 constitute a bias control circuit 63.

[0053] Incidentally, since other elements of structure in Fig. 6 are similar to those employed in the embodiment 1, description on them will be omitted. However, the bias applying circuit 25 subtracts the current supplied to the current subtracting circuit 62 from a reference current and applies a bias corresponding to the post-subtraction remaining current to each bases of transistors 12-1 to 12-N.

[0054] An example illustrative of configurations of the detection adjusting circuit 61 and the current subtracting circuit 62 where N type bipolar transistors are used as the transistors 12-1 to 12-N, are shown hereinafter. Fig. 7 is a circuit diagram showing the configurations of detection adjusting circuit 61 and the current subtracting circuit 62 shown in Fig. 6. In the figure, reference numeral 71 indicates a variable resistor, and 72 indicates apower supply, respectively. Designated at numerals 81 and 82 are respectively N type transistors which constitute a current mirror circuit whose one end is connected to the detection adjusting circuit 61 and whose other end is connected to the bias applying circuit 25. Incidentally, the bias applying circuit 25 in this case may make use of one shown in Fig. 5.

[0055] The operation will next be explained.

[0056] Since the high-frequency amplifying unit 2 is operated in a manner similar to the embodiment 1, the description thereof will be omitted.

[0057] The detection circuit 21 detects a high-frequency signal supplied via an input terminal 1 and supplies the post-detection signal to the smoothing circuit 22. The smoothing circuit 22 smoothes the signal. Incidentally, the detection adjusting circuit 61 connected to the smoothing circuit 22 adjusts a current passing through the detector circuit 21 and the smoothing circuit 22. The current subtracting circuit 62 causes the bias applying circuit 25 to supply a current of value corresponding to the amplitude of input signal through based on the current adjusted by the detection adjusting circuit 61. The bias applying circuit 25 subtracts the current supplied to the current subtracting circuit 62 from a reference current and applies a bias corresponding to the so-subtracted remaining current to each bases of transistors 12-1 to 12-N. Thus when the amplitude of input signal increases, the post-subtraction remaining current decreases and the bias applied to each bases of transistors 12-1 to 12-N is reduced. On the other hand, when the amplitude of input signal decreases, the post-subtraction remaining current increases and the bias applied to each bases of transistors 12-1 to 12-N becomes large.

[0058] A description will now be made for operation when the respective parts are configured as shown in Figs. 5 and 7.

[0059] First, the detector circuit 21 and the smoothing circuit 22 extract the voltage amplitude of an input signal and allow a current corresponding to the voltage amplitude of input signal to conduct into the N type transistor 81 of current mirror circuit, based on the resistance value of variable resistor 71 and the voltage of power supply 72. Thus a current obtained by multiplying the current by a ratio between junction areas of the N type transistors 81 and 82 is allowed to conduct into the N type transistor 82 of current mirror circuit (see Fig. 7). At this time, the current which passes through the N type transistor 82, is conducted from the bias applying circuit 25 to the current subtracting circuit 62.

[0060] In the bias applying circuit 25, a reference bias for the N type transistor 51 is determined according to a voltage from the power supply 53, a resistance value of the resistor 52 and an emitter-to-base voltage of the N type transistor 54 when no current is supplied to the current subtracting circuit 62. A reference current corresponding to the reference bias serves so as to make continuity between the collector and emitter. When the current is supplied to the current subtracting circuit 62,

the current is subtracted from the reference current, and thereafter the post-subtraction remaining current flows into the collector of N type transistor 51 of the bias applying circuit 25. The bias applied to the base of N type transistor 51 also varies according to a change in the emitter-to-collector current. Since the N type transistor 51 constitutes the current mirror circuit together with the transistors 12-1 to 12-N of high-frequency amplifying unit 2, the bias applied to each bases of transistors 12-1 to 12-N of the high-frequency amplifying unit 2 also changes in the same manner as described above (see Fig. 5).

[0061] Thus the detector circuit 21, the smoothing circuit 22, the detection adjusting circuit 61, the current subtracting circuit 62 and the bias applying circuit 25 continuously adjust the bias for each transistors 12-1 to 12-N of high-frequency amplifying unit 2 according to the amplitude of input signal.

[0062] Thus according to the embodiment 2, an effect is obtained that a steep gain variation produced according to a change in the amplitude of input high-frequency signal can be suppressed since the high-frequency amplifying unit 2 having the plurality of transistors 12-1 to 12-N for amplifying the input high-frequency signal, the measuring circuit 27 for measuring the amplitude of input high-frequency signal, and the bias control circuit 63 for continuously controlling the bias applied to each transistors 12-1 to 12-N according to the value of amplitude measured by the measuring circuit 27 are provided.

[0063] According to the embodiment 2 as well, an effect is obtained that the circuit scale can be reduced since the bias control circuit 63 collectively controls the bias applied to each plurality of transistors 12-1 to 12-N.

[0064] Further according to the embodiment 2, an effect is obtained that the bias can be increased continuously when the amplitude of input high-frequency signal is reduced, thus it makes possible to compensate for a gain reduction at low output power since the bias control circuit 63 has the current subtracting circuit 62 for inputting the current having a value corresponding to the amplitude measured by the measuring circuit 27, and the bias applying circuit 25 for supplying the current to the current subtracting circuit and applying the bias corresponding to the difference between a predetermined reference current and the current to a plurality of amplifying elements. That is to say, when it is necessary to compensate for a gain reduction at low output power according to the type of device used in each transistors 12-1 to 12-N, the bias control circuit 63 is used, whereas when it is necessary to reduce power consumption at low output power, the bias control circuit 26 is used.

[0065] Furthermore according to the embodiment 2, an effect is obtained that the operating condition (operating point of the diode constituting the detector circuit 21) for the measuring circuit 27 can be controlled and hence an adjustment of the device can be easily performed since the bias control circuit 63 has the detection adjusting circuit 61 for setting a value of current conducted according to the amplitude of high-frequency signal when the measuring circuit 27 measures the amplitude thereof.

[0066] Still further according to the embodiment 2, an effect is obtained that the characteristic of current from the bias applying circuit 25 with respect to the amplitude of input high-frequency signal can easily be adjusted by setting the ratio between the junction areas of current mirror circuit and the source voltage thereof, and in its turn the bias applied to each transistors 12-1 to 12-N can be adjusted with ease since the current subtracting circuit 62 has the current mirror circuit for allowing the current of value corresponding to the amplitude measured by the measuring circuit 27 to conduct into one end thereof and according to the current, causing another current set based on the ratio between the junction areas of the current mirror circuit and the source voltage thereof to be inputted from the other end thereof.

[0067] Still further according to the embodiment 2, an effect is obtained that the measuring circuit 27 is capable of measuring the amplitude of high-frequency signal without degradation of the high-frequency signal supplied to the high-frequency amplifying unit 2 since the measuring circuit 27 is connected in parallel with the high-frequency amplifying unit 2.

[0068] Still further according to the embodiment 2, an effect is obtained that the measuring circuit 27, the detection adjusting circuit 61 and the current subtracting circuit 62 can be implemented in a one-chip integrated circuit, thus it makes possible to reduce the scale and cost of the device since the measuring circuit 27, the detection adjusting circuit 61 and the current subtracting circuit 62 are connected in parallel with the high-frequency amplifying unit 2.

Embodiment 3

[0069] Fig. 8 is a block diagram showing a configuration of high-frequency amplifying device according to an embodiment 3 of the present invention. In the high-frequency amplifying device according to the embodiment 3, N pieces of bias control circuits 26 are respectively connected to N pieces of transistors 12-1 to 12-N. Incidentally, since other configurations and configurations of the respective bias control circuits 63 in Fig. 8 are similar to those employed in the embodiment 1, description on them will be omitted.

[0070] The operation will next be explained.

[0071] In the high-frequency amplifying device according to the embodiment 3, the bias control circuits 26 provided at respective stages independently apply biases to respective transistors 12-i (where i = 1,..., N) respectively. At this time, the respective biases are set in consideration of, for example, the frequency characteristics and physical characteristics of the respective transistors 12-i, etc. Incidentally, since the respective parts are similar in operation to those employed in the embodiment 1, the description thereof will be omitted.

[0072] Thus according to the embodiment 3, an effect is obtained that the biases can be set independently according to the frequency characteristics and physical characteristics of the respective transistors 12-i since there are provided a high-frequency amplifying unit 2 having the plurality of transistors 12-1 to 12-N for amplifying an input high-frequency signal, a measuring circuit 27 for measuring the amplitude of input high-frequency signal, and a plurality of the bias control circuits 26 for respectively independently controlling the biases applied to the respective transistors 12-i continuously according to the value of amplitude measured by the measuring circuit 27.

[0073] According to the embodiment 3 as well, since each bias control circuits 26 has a current adding circuit 24 for outputting a current corresponding to the amplitude measured by the measuring circuit 27, and a bias applying circuit 25 for applying a bias corresponding to the sum of current supplied from the current adding circuit 24 and a predetermined reference current to any of the transistors 12-1 to 12-N, an effect similar to the effect obtained in the embodiment 1 is obtained. Further, an effect is obtained that the biases applied to the respective transistors 12-i can be set independently and power consumption at low output power can be further reduced.

Embodiment 4

[0074] Fig. 9 is a block diagram showing a configuration of high-frequency amplifying device according to an embodiment 4 of the present invention. In the high-frequency amplifying device according to the embodiment 4, N bias control circuits 63 are respectively connected to N transistors 12-1 to 12-N. Incidentally, since other configurations and configurations of the respective bias control circuits 63 in Fig. 9 are similar to those employed in the embodiment 2, description on them will be omitted.

[0075] The operation will next be explained.

[0076] In the high-frequency amplifying device according to the embodiment 4, the bias control circuits 63 provided at respective stages independently apply biases to respective transistors 12-i (where i = 1, ..., N) respectively. At this time, the respective biases are set in consideration of, for example, the frequency characteristics and physical characteristics of the respective transistors 12-i, etc. Incidentally, since the respective parts are similar in operation to those employed in the embodiment 2, the description thereof will be omitted.

[0077] Thus according to the embodiment 4, an effect is obtained that the biases can be set independently according to the frequency characteristics and physical characteristics of the respective transistors 12-i since there are provided a high-frequency amplifying unit 2 having the plurality of transistors 12-1 to 12-N for amplifying an input high-frequency signal, a measuring circuit 27 for measuring the amplitude of input high-frequency signal, and a plurality of the bias control circuits 63 for respectively independently controlling the biases applied to the respective transistors 12-i continuously according to the value of amplitude measured by the measuring circuit 27.

[0078] According to the embodiment 4 as well, since each bias control circuits 63 has a current subtracting circuit 62 for inputting a current corresponding to the amplitude measured by the measuring circuit 27, and a bias applying circuit 25 for supplying the current to the current subtracting circuit 62 and applying a bias corresponding to the difference between a predetermined reference current and the current to each amplifying element, an effect similar to the effect obtained in the embodiment 2 is obtained. Further, an effect is obtained that the biases applied to the respective transistors 12-i can be set independently and the compensation for a gain reduction at low output power can be carried out more suitably.

Embodiment 5

[0079] Fig. 10 is a block diagram showing a configuration of high-frequency amplifying device according to an embodiment 5 of the present invention. In the high-frequency amplifying device according to the embodiment 5, bias control circuits 26 and bias control circuits 63 equal to N in total are respectively connected to N transistors 12-1 to 12-N. Incidentally, since other configurations and configurations of the respective bias control circuits 26 and 63 in Fig. 10 are similar to those employed in the embodiment 1 or embodiment 2, description on them will be omitted.

[0080] Incidentally, while the bias control circuit 63 is used in a first stage and the bias control circuits 26 are used in an (N-1)th stage and an Nth stage in Fig. 10, the combination of these is not limited to the above in particular. The bias control circuits 26 and the bias control circuits 63 may be used even by any number.

[0081] The operation will next be explained.

[0082] In the high-frequency amplifying device according to the embodiment 5, the bias control circuits 63 are provided for transistors 12-1 to 12-M of predetermined M stages on the front side, and the bias control circuits 26 are provided for transistors 12-(M-1) to 12-N of the remaining (N-M) stages. Thus biases are independently applied to their corresponding transistors 12-i (where i = 1, ..., N). At this time, the respective biases are set in consideration of, for example, the frequency characteristics and physical characteristics of the transistors 12-i, etc. Incidentally, since the respective parts are similar in operation to those employed in the embodiment 1 or embodiment 2, the description thereof will be omitted.

[0083] Thus according to the embodiment 5, an effect is obtained that the transistors 12-1 to 12-M used as drivers, for example, compensate for a gain reduction, and the transistors 12-(M+1) to 12-N used as power am-

plifiers, for example, reduce power consumption, whereby a reduction in distortion and a reduction in power consumption can be rendered compatible since the predetermined number of stages of bias control circuits 63 on the front side, of the plurality of bias control circuits 26 and 63 respectively have current subtracting circuits 62 for respectively inputting thereto a current of value corresponding to amplitude measured by a measuring circuit 27, and bias applying circuits 25 for respectively supplying the current to the current subtracting circuits 62 and applying biases each corresponding to the difference between a predetermined reference current and the current to their corresponding transistors 12-i (where i = 1, ..., M), and the remaining bias control circuits 26 on the rear side respectively have current adding circuits 24 for respectively outputting the current of value corresponding to the amplitude measured by the measuring circuit 27, and bias applying circuits 25 for respectively applying biases each corresponding to the sum of the current supplied from each current adding circuit 24 and the predetermined reference current to their corresponding transistors 12-i (where i = M+1, ..., N).

Embodiment 6

[0084] Fig. 11 is a block diagram showing a configuration of high-frequency amplifying device according to an embodiment 6 of the present invention. Fig. 12 is a circuit diagram showing an example of configuration of a detector circuit 91 shown in Fig. 11. In the figure, reference numeral 91 indicates a detector circuit for passing a high-frequency signal to a high-frequency amplifying unit 2 and detecting the high-frequency signal. In the detector circuit 91, reference numeral 101 indicates a capacitor connected to an input terminal 1, for allowing the high-frequency signal to pass through and suppressing a dc component or the like, 102 indicates a capacitor connected to the high-frequency amplifying unit 2, for allowing the high-frequency signal to pass through and suppressing a dc component or the like, 103 indicates a detecting diode, and 104 indicates an inductor for suppressing a high-frequency component to the smoothing circuit 22. Incidentally, since other elements of structure shown in Fig. 11 are respectively similar to those employed in the embodiment 1, the description thereof will be omitted.

[0085] The operation will next be explained.

[0086] The detector circuit 91 supplies the input high-frequency signal to the high-frequency amplifying unit 2 through the capacitors 101 and 102. Incidentally, the high-frequency signal inputted thereto at this time is cut or blocked off by the inductor 104 and is hence not supplied to the smoothing circuit 22. On the other hand, since a component of the input high-frequency signal, which is detected by the diode 103, is of a low frequency, it is supplied to the smoothing circuit 22 through the inductor 104. Incidentally, since other operations are similar to those in the embodiment 1, the description thereof will be omitted.

[0087] Thus according to the embodiment 6, an effect is obtained that it is unnecessary to additionally provide a divider for allowing the high-frequency signal to divide into the measuring circuit 27 and high-frequency amplifying unit 2, thus it makes possible to reduce a circuit scale since the detector circuit 91 is connected in series with the high-frequency amplifying unit 2 and passes the high-frequency signal to the high-frequency amplifying unit 2, and detects the high-frequency signal.

[0088] Incidentally, while the embodiment 6 is one wherein the detector circuit 21 employed in the embodiment 1 is changed to the detector circuit 91, each detector circuits 21 employed in the embodiments 2 through 5 maybe changed to the detector circuit 91. Even in this case, an effect similar to the above is obtained.

[0089] Incidentally, while the above-described embodiment has explained the case in which N type bipolar transistors are used as amplifying elements for the high-frequency amplifying unit 2 by way of example, other types of transistor or the like such as field effect transistor may be used as the amplifying elements for the high-frequency amplifying unit 2. In such a case, however, internal circuit configurations of bias control circuits 26 and 63 must be modified correspondingly.

INDUSTRIAL APPLICABILITY

[0090] As described above, the present invention is suitable to use in amplification of the high-frequency signal in, for example, a communication apparatus for transmitting and receiving a high-frequency signal

Claims

1. A high-frequency amplifying device for amplifying a high-frequency signal with a plurality of stages of amplifying elements, comprising:

   a high-frequency amplifying unit having a plurality of the amplifying elements for amplifying the input high-frequency signal;
   a measuring circuit for measuring amplitude of said input high-frequency signal; and
   a bias control circuit for continuously controlling a bias applied to each of said amplifying elements according to value of said amplitude measured by said measuring circuit.

2. The high-frequency amplifying device according to claim 1, wherein said bias control circuit has a current adding circuit for outputting a current having a value corresponding to the amplitude measured by said measuring circuit, and a bias applying circuit for applying a bias corresponding to the sum of current output from the current adding circuit and a pre-

determined reference current to the plurality of amplifying elements.

3. The high-frequency amplifying device according to claim 2, wherein said bias control circuit has a detection adjusting circuit for setting value of a current conducted according to said amplitude of the high-frequency signal when said measuring circuit measures the amplitude thereof.

4. The high-frequency amplifying device according to claim 2, wherein said current adding circuit has a current mirror circuit for allowing a current having a value corresponding to the amplitude measured by said measuring circuit to conduct into one end thereof and according to the current, outputting another current set based on a ratio between junction areas of the current mirror circuit and a source voltage from the other end thereof.

5. The high-frequency amplifying device according to claim 2, wherein said bias applying circuit has an internal amplifying element for conducting the current output from the current adding circuit and the predetermined reference current, and said internal amplifying element and the plurality of amplifying elements of said high-frequency amplifying unit constitute a current mirror circuit.

6. The high-frequency amplifying device according to claim 1, wherein said bias control circuit has a current subtracting circuit for inputting thereto a current having a value corresponding to the amplitude measured by said measuring circuit, and a bias applying circuit for supplying the current to the current subtracting circuit and applying a bias corresponding to a difference between a predetermined reference current and said current to the plurality of amplifying elements.

7. The high-frequency amplifying device according to claim 6, wherein said bias control circuit has a detection adjusting circuit for setting a value of current conducted according to the amplitude of high-frequency signal when said measuring circuit measures the amplitude thereof.

8. The high-frequency amplifying device according to claim 6, wherein said current subtracting circuit has a current mirror circuit for allowing a current having a value corresponding to the amplitude measured by said measuring circuit to conduct into one end thereof and according to the current, inputting another current set based on a ratio between junction areas of the current mirror circuit and a source voltage from the other end thereof.

9. The high-frequency amplifying device according to claim 6, wherein said bias applying circuit has an internal amplifying element for conducting the remaining current obtained by subtracting the current supplied to the current subtracting circuit from the predetermined reference current, and

the internal amplifying element and the plurality of amplifying elements of said high-frequency amplifying unit constitute a current mirror circuit.

10. The high-frequency amplifying device according to claim 1, wherein said measuring circuit is connected in parallel with said high-frequency amplifying unit.

11. The high-frequency amplifying device according to claim 3, wherein said measuring circuit, said current adding circuit and said detection adjusting circuit are connected in parallel with said high-frequency amplifying unit.

12. The high-frequency amplifying device according to claim 7, wherein said measuring circuit, said current subtracting circuit and said detection adjusting circuit are connected in parallel with said high-frequency amplifying unit.

13. The high-frequency amplifying device according to claim 1, wherein said measuring circuit has a detector circuit connected in series with said high-frequency amplifying unit, for passing the high-frequency signal to said high-frequency amplifying unit and detecting the high-frequency signal.

14. A high-frequency amplifying device for amplifying a high-frequency signal with a plurality of stages of amplifying elements, comprising:

a high-frequency amplifying unit having a plurality of the amplifying elements for amplifying the input high-frequency signal;
a measuring circuit for measuring the amplitude of input high-frequency signal; and
a plurality of bias control circuits for respectively independently controlling continuously biases applied to the respective amplifying elements according to the value of amplitude measured by said measuring circuit.

15. The high-frequency amplifying device according to claim 14, wherein each of said bias control circuits has a current adding circuit for outputting a current having a value corresponding to the 1amplitude measured by said measuring circuit, and a bias applying circuit for applying a bias corresponding to the sum of current output from the current adding circuit and a predetermined reference current to said each amplifying element.

16. The high-frequency amplifying device according to claim 14, wherein each of said bias control circuit has a current subtracting circuit for inputting thereto a current having a value corresponding to the amplitude measured by said measuring circuit, and a bias applying circuit for supplying the current to said current subtracting circuit and applying a bias corresponding to the difference between a predetermined reference current and the current to said each amplifying element.

17. The high-frequency amplifying device according to claim 14, wherein each of said bias control circuit of a predetermined number of stages on the front side, of said plurality of bias control circuits has a current subtracting circuit for inputting thereto a current having a value corresponding to the amplitude measured by said measuring circuit, and a bias applying circuit for supplying the current to the current subtracting circuit and applying a bias corresponding to the difference between a predetermined reference current and the supplied current to said each amplifying element, and each of said remaining bias control circuits on the rear side has a current adding circuit for outputting a current having a value corresponding to the amplitude measured by said measuring circuit, and a bias applying circuit for applying a bias corresponding to the sum of current output from the current adding circuit and a predetermined reference current to said each amplifying element.

FIG.1

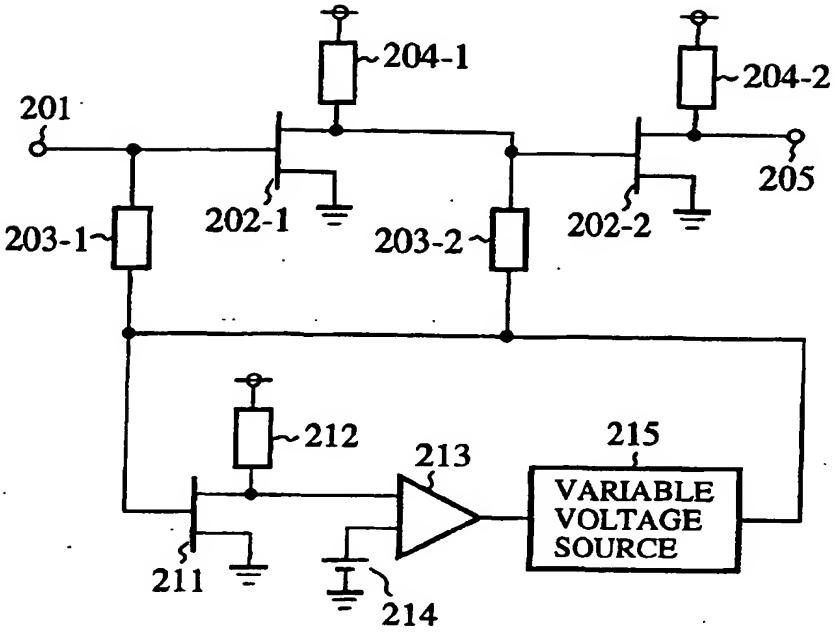


FIG.3

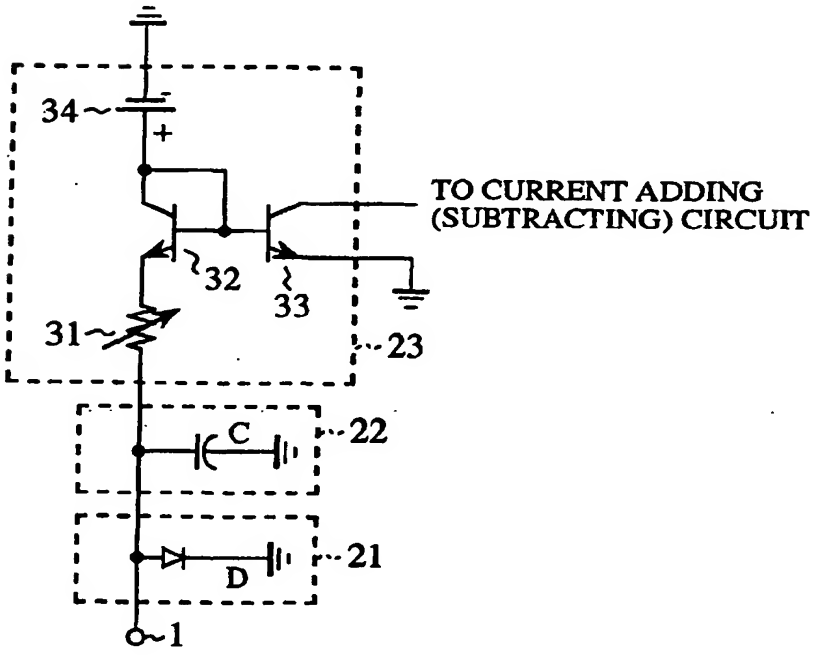


FIG.2

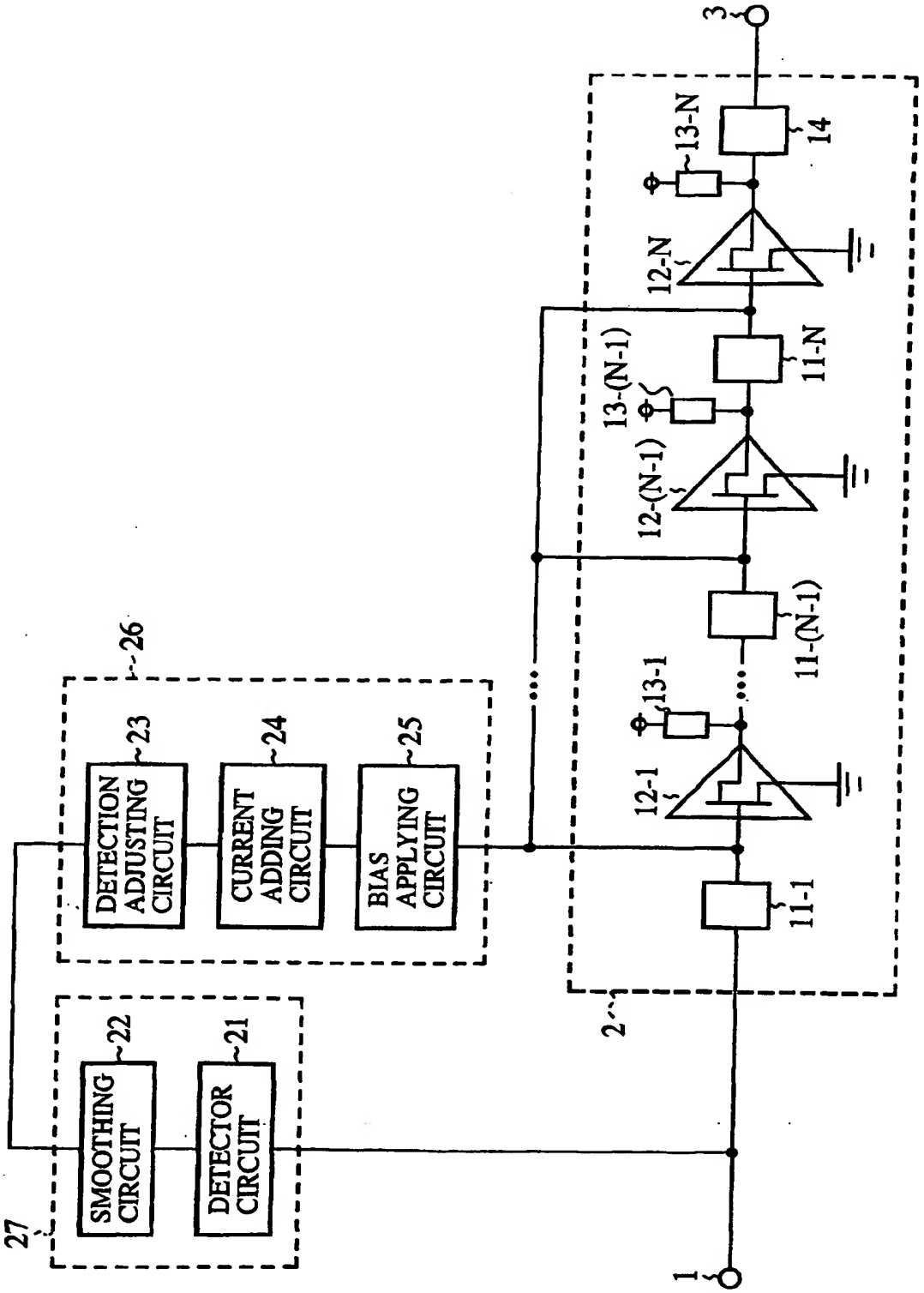


FIG.4

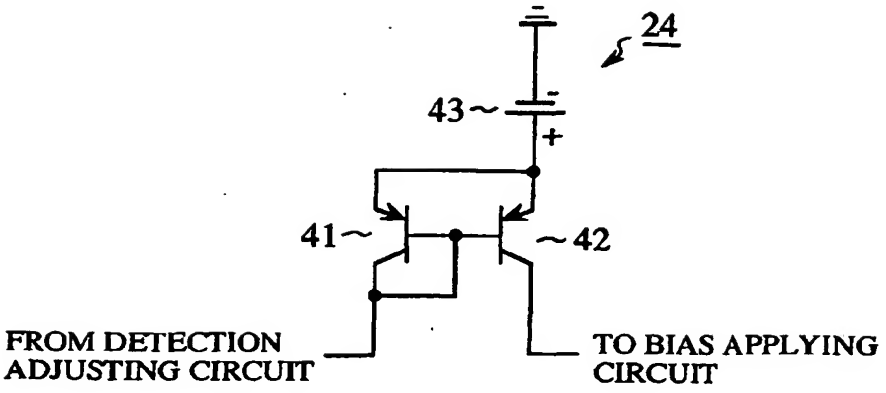


FIG.5

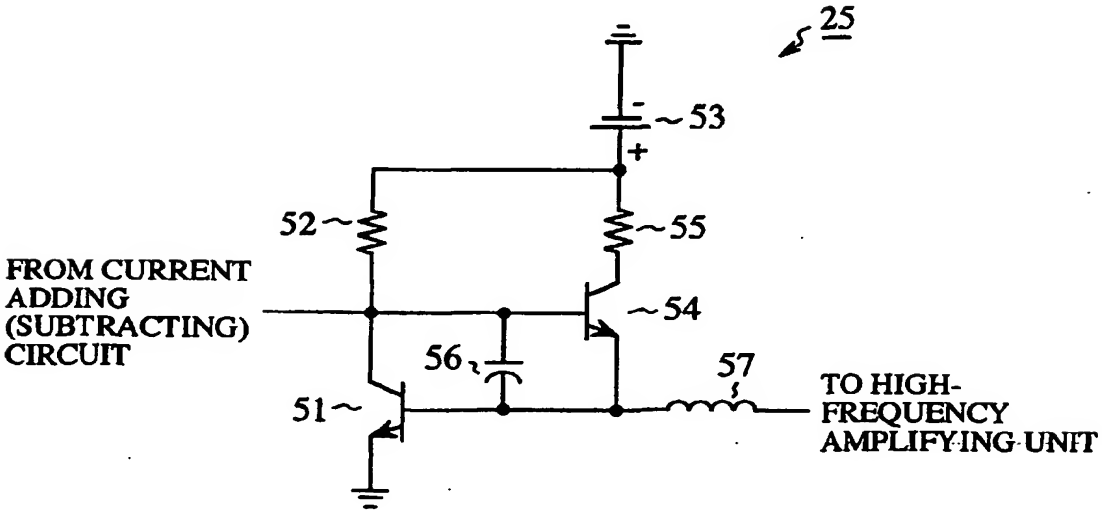


FIG.6

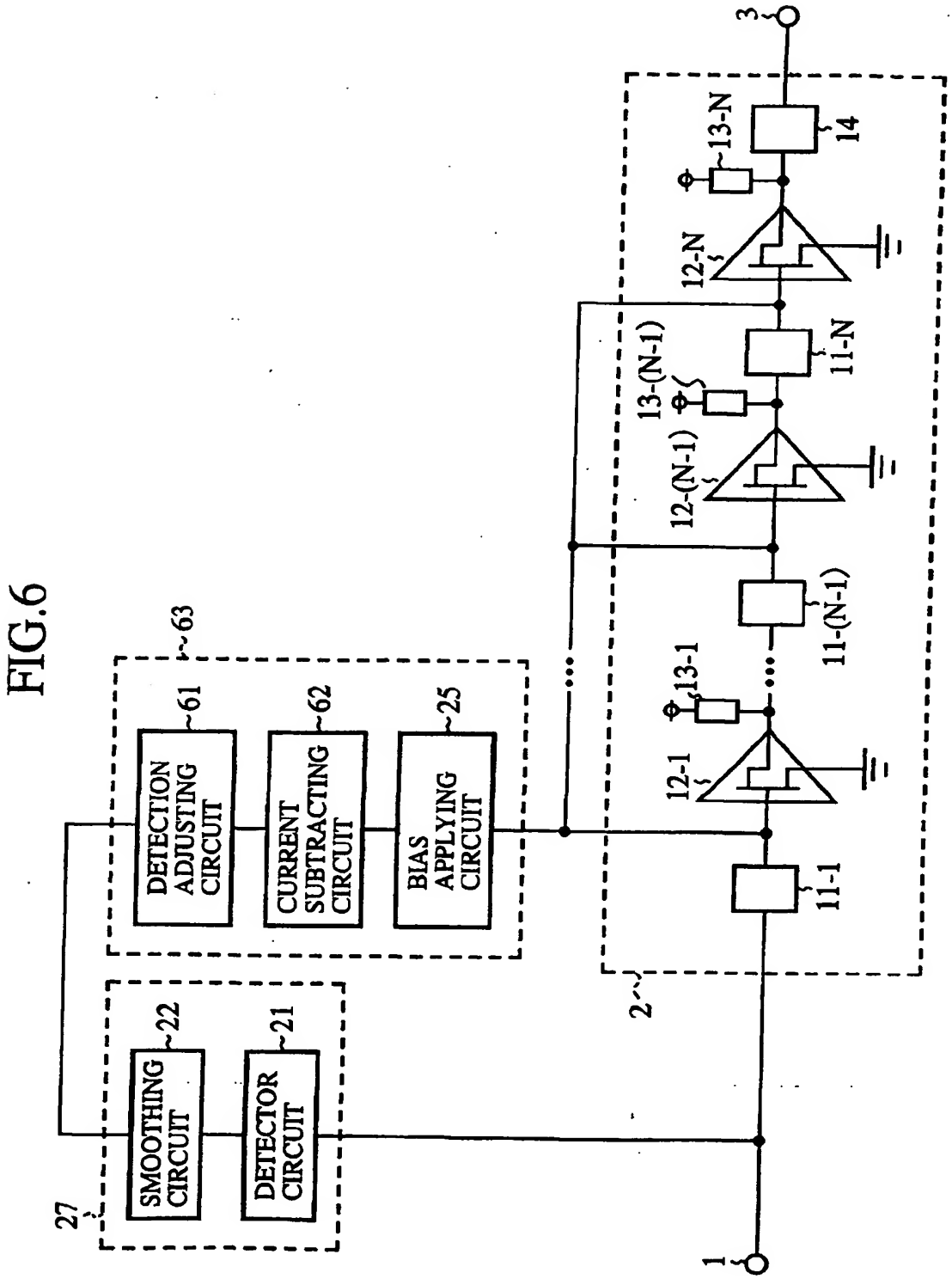


FIG.7

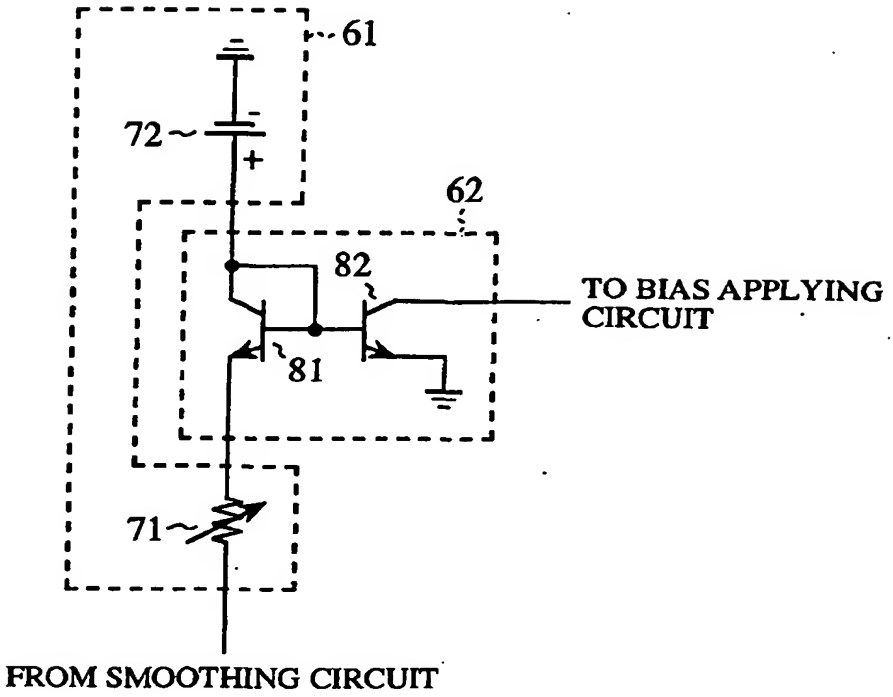


FIG.12

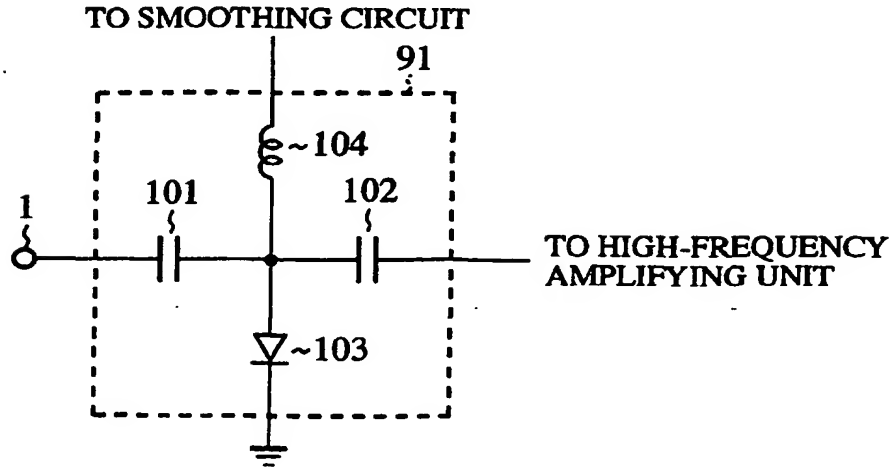


FIG.8

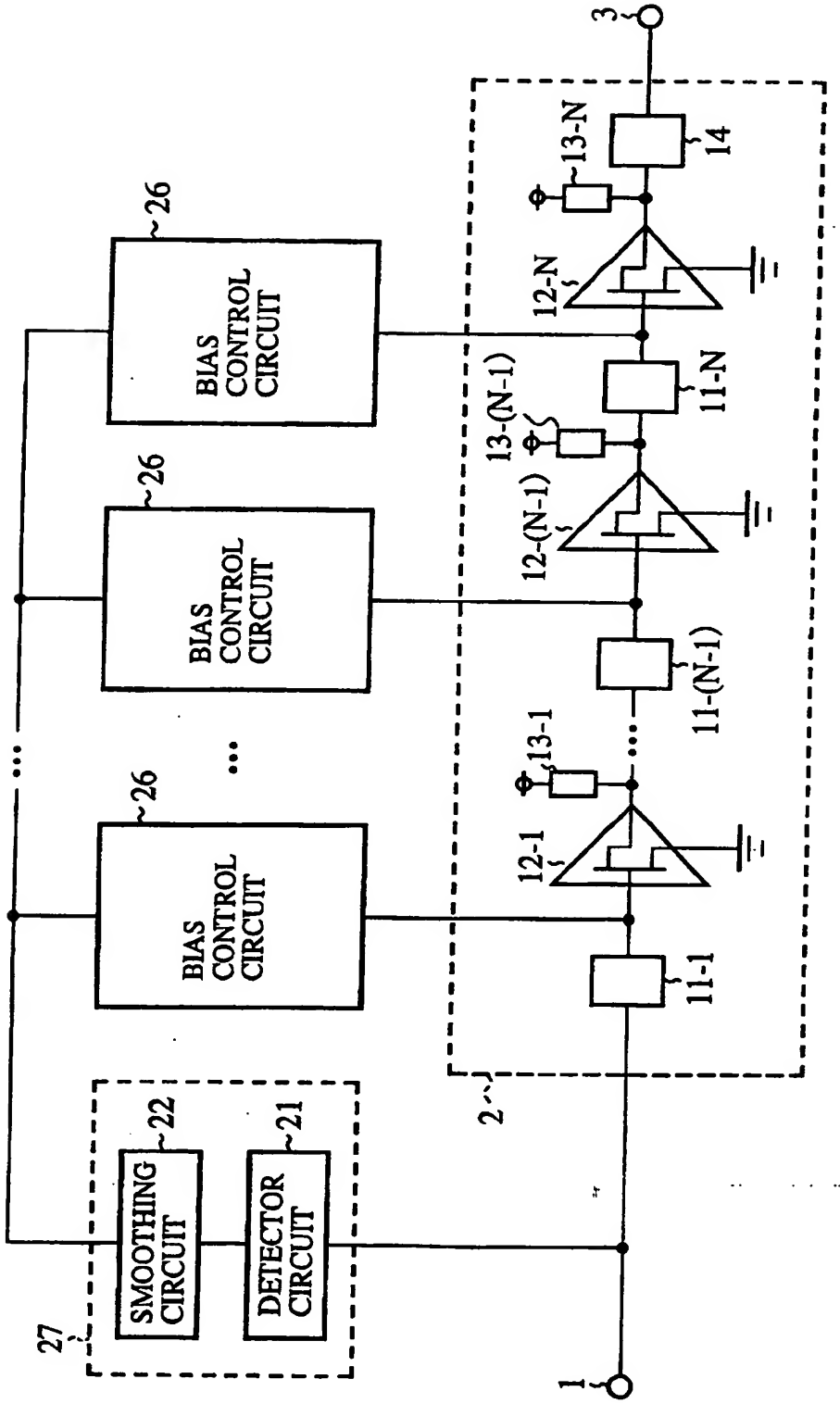


FIG.9

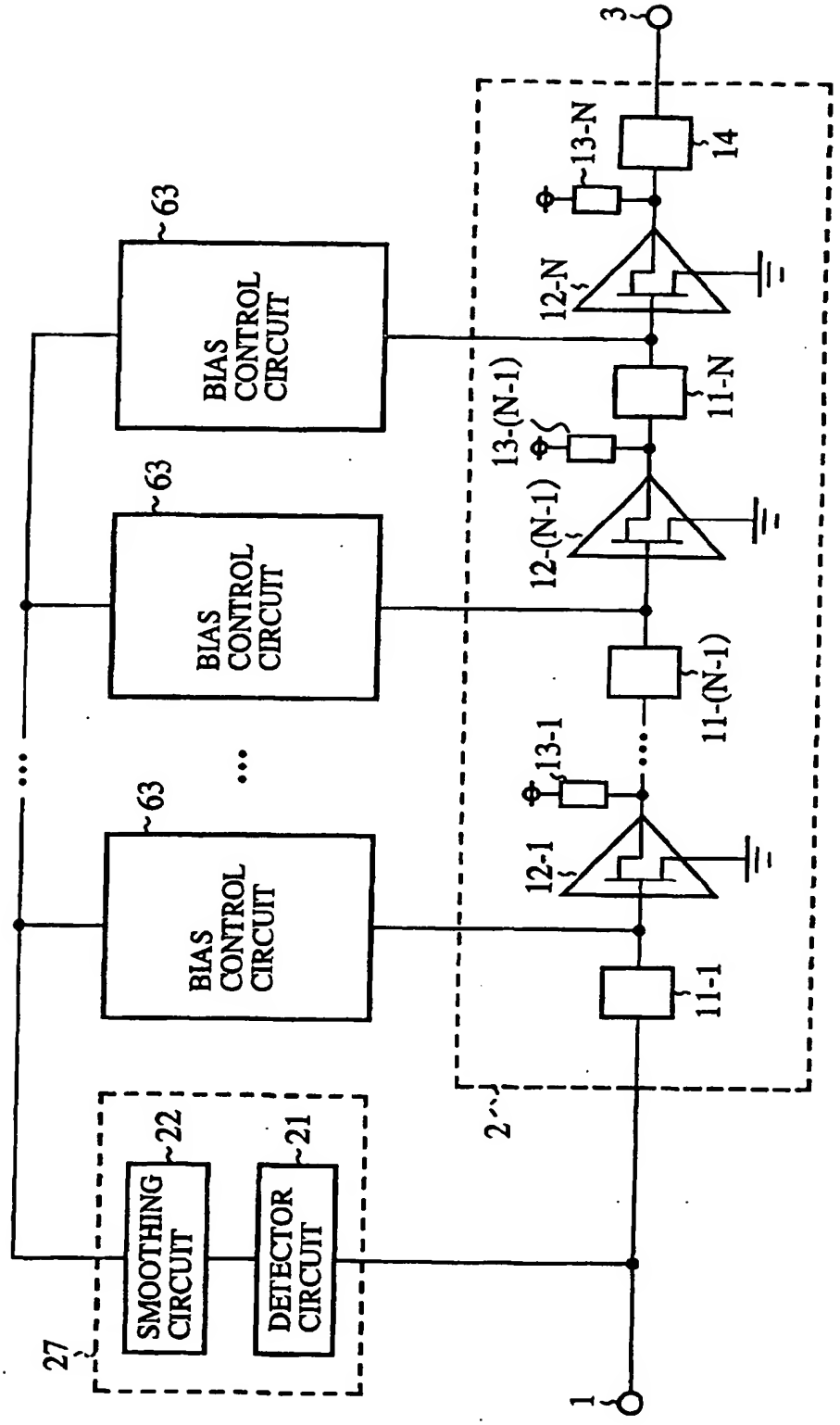


FIG.10

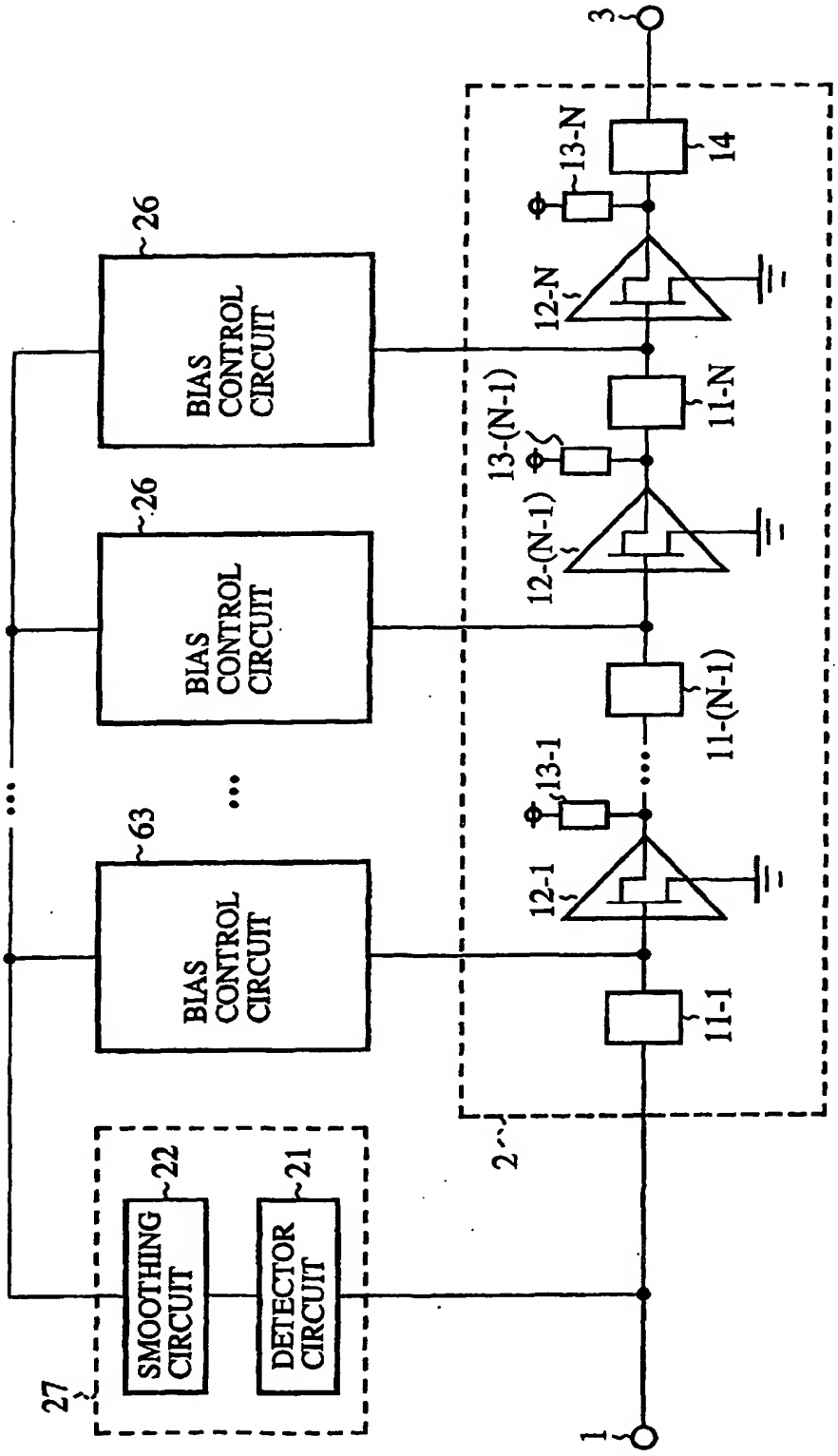
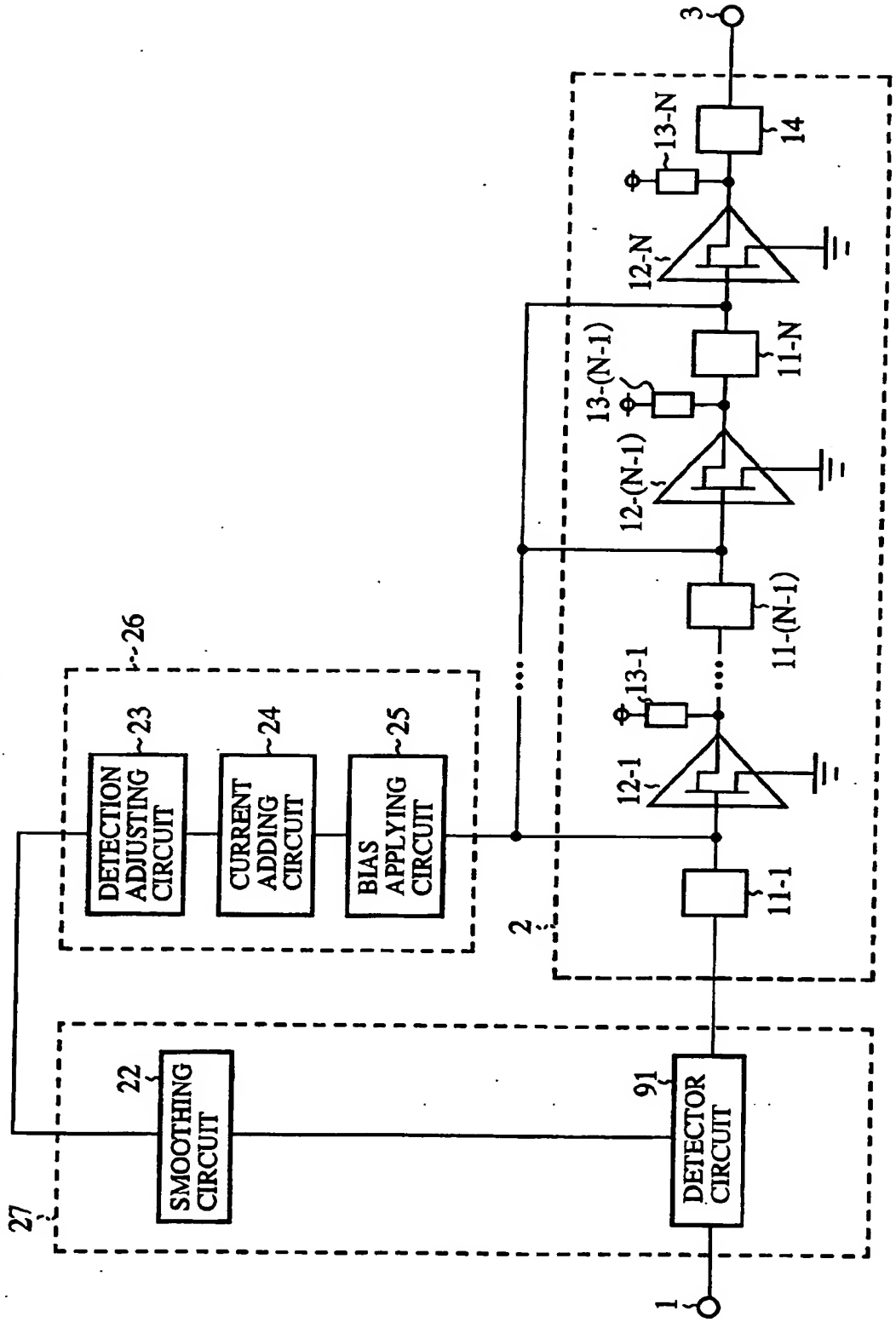


FIG.11



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP01/05667

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl.[7] H03F 3/19

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl.[7] H03F 3/19, 1/02, 1/32

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Toroku Jitsuyo Shinan Koho 1994-2001
Kokai Jitsuyo Shinan Koho 1971-2001 Jitsuyo Shinan Toroku Koho 1996-2001

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 62-274906 A (Nippon Telegr. & Teleph. Corp. <NTT>), 28 November, 1987 (28.11.87), Full text (Family: none)	1-17
A	JP 56-80906 A (Hitachi, Ltd.), 02 July, 1981 (02.07.81), Full text (Family: none)	1-17
A	JP 09-270650 A (Alps Electric Co., Ltd.), 14 October, 1997 (14.10.97), Full text & GB 2311670 A & FR 2746984 A	1-17

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 September, 2001 (25.09.01)	16 October, 2001 (16.10.01)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)